WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first circuit block supplied with a first operating voltage;

a second circuit block supplied with a second operating voltage;

a voltage generating circuit for generating a third operating voltage in response to said first operating voltage; and

a third circuit block supplied with said third operating voltage.

2. A semiconductor device according to Claim 1, wherein said first operating voltage is higher than said second operating voltage.

3. A semiconductor device according to Claim 2, wherein said third operating voltage is lower than said first operating voltage.

4. A semiconductor device according to Claim 1, wherein said voltage generating circuit includes a first voltage conversion circuit for generating a fourth operating voltage higher than said first operating voltage in response to said first operating voltage, and a second voltage conversion circuit for generating said third operating voltage in response to said fourth operating voltage.

5. A semiconductor device according to Claim 4, further comprising a reference voltage generating circuit for generating a reference voltage,

said first voltage conversion circuit including a charge pump circuit having a voltage-increasing capacitor excited by a cyclic pulse signal;

said second voltage conversion circuit including a voltage down-converter for dropping said fourth operating voltage on the basis of said reference voltage to thereby generate said third operating voltage.

6. A semiconductor device according to Claim 1, wherein:

said semiconductor device is a semiconductor integrated circuit formed on a semiconductor chip;

said first circuit block includes an input/output circuit for inputting/outputting a signal from/to an outside of said semiconductor chip;

said second circuit block includes a logic circuit for receiving said signal input through said first circuit block and outputting a predetermined result to said first circuit block;

said third circuit block includes a dynamic memory composed of a plurality of dynamic memory cells provided at intersection points between a plurality of word lines and a plurality of bit lines, and a word line drive circuit for driving selected one of said word lines with said third operating voltage;

said dynamic memory is arranged so that information stored in one of said dynamic memory cells corresponding to an address signal issued from said

logic circuit of said second circuit block is sent out to said logic circuit;

said first and second operating voltages are supplied from an outside of said semiconductor chip; and

said first operating voltage is higher than each of said second and third operating voltages.

7. A semiconductor device according to Claim 6, wherein said voltage generating circuit includes a voltage up-converter for generating a fourth operating voltage higher than said first operating voltage in response to said first operating voltage, and a voltage down-converter for generating said third operating voltage lower than said fourth operating voltage.

8. A semiconductor device according to Claim 6, wherein:

signal input/output between said first and second circuit blocks is performed through a first level conversion circuit for converting a first signal with an amplitude of said first operating voltage into a second signal with an amplitude of said second operating voltage and a second level conversion circuit for converting a third signal with an amplitude of said second operating voltage into a fourth signal with an amplitude of said first operating voltage; and

signal input/output between said second and third circuit blocks is performed under an amplitude of said second operating voltage.

9. A semiconductor device according to Claim 1,

wherein said semiconductor device is a semiconductor integrated circuit formed on a semiconductor chip and further comprises:

a first power supply terminal for receiving said first operating voltage from the outside of said semiconductor chip;

a first power supply wiring pattern connected to said first power supply terminal;

a second power supply terminal for receiving said second operating voltage from the outside of said semiconductor chip;

a second power supply wiring pattern connected to said second power supply terminal;

a third power supply terminal for receiving a reference electric potential for said first operating voltage from the outside of said semiconductor chip;

a third power supply wiring pattern connected to said third power supply terminal;

a fourth power supply terminal for receiving a reference electric potential for said second operating voltage from the outside of said semiconductor chip; and

a fourth power supply wiring pattern connected to said fourth power supply terminal, and wherein:

said third and fourth power supply wiring patterns are separated from each other on said semiconductor chip;

said first circuit block and said voltage generating circuit are supplied with said first

operating voltage through said first and third power supply wiring patterns; and

said second circuit block is supplied with said second operating voltage through said second and fourth power supply wiring patterns.

10. A semiconductor device according to Claim 1, wherein said semiconductor device is a semiconductor integrated circuit formed on a semiconductor chip and further comprises:

a first power supply terminal for receiving said first operating voltage from the outside of said semiconductor chip;

a first power supply wiring pattern connected to said first power supply terminal;

a second power supply terminal for receiving said second operating voltage from the outside of said semiconductor chip;

a second power supply wiring pattern connected to said second power supply terminal;

a third power supply terminal for receiving a common reference electric potential for said first and second operating voltages from the outside of said semiconductor chip;

a third power supply wiring pattern connected to said third power supply terminal, and wherein:

said first circuit block and said voltage generating circuit are supplied with said first operating voltage through said first and third power

supply wiring patterns; and

said second circuit block is supplied with said second operating voltage through said second and third power supply wiring patterns.

11. A semiconductor device according to Claim 1, wherein said semiconductor device is a semiconductor integrated circuit formed on a semiconductor chip and further comprises:

a first power supply terminal for receiving said first operating voltage from the outside of said semiconductor chip;

a first power supply wiring pattern connected to said first power supply terminal for supplying said first operating voltage to said first circuit block;

a second power supply terminal for receiving said second operating voltage from the outside of said semiconductor chip;

a second power supply wiring pattern connected to said second power supply terminal for supplying said second operating voltage to said second circuit block;

a third power supply terminal disposed separately from said first power supply terminal for receiving said first operating voltage from the outside of said semiconductor chip;

a third power supply wiring pattern connected to said third power supply terminal for supplying said first operating voltage to said voltage generating circuit, and wherein:

said first and third power supply wiring patterns are separated from each other on said semiconductor chip.